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Application of Silicon Rich Oxide Films in New Optoelectronic Devices

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The optoelectronic properties of new metal-insulator-silicon (MIS) optical sensors are described. Silicon rich oxide layer is used as an insulator in this sensor. We are discussing the case when applied voltage bias is not enough for significant thorough leakage current through the silicon rich oxide layer. At that, the sensor presents a MIS capacitor, photoelectric properties of which are investigated and simulated numerically. It is shown that at stepped voltage bias the sensor operates in two quasi-equilibrium modes. A transition between these modes presents a practical interest. In the first operating mode, photo generated minority carriers are stored in the potential well at silicon rich oxide/silicon interface. The readout of stored charge occurs at stepped changing the applied voltage bias. At that, the inversion charge is injected into the silicon substrate and a displacement current peak is obtained. The amplitude of this peak exceeds drastically the value of photocurrent at the storing stage. An internal amplification coefficient of current exceeds the value of 10^4. Thus, the investigated sensors have an internal amplification of the electrical signal and they can be used for a weak optical signal registration. Numerical model has been put forward, where a presence of inversion and depletion regions in semiconductor, and also a leakage through the silicon rich oxide are taken into account. Simulations have been done for experimental input parameters and demonstrate a good agreement with the experimental results.

Keywords: optical sensor, metal-insulator-semiconductor capacitor, transient, internal gain.

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I. Introduction

Non-stoichiometric silicon oxides (or Silicon Rich Oxide, SRO) are a variation of silicon dioxide (SiO_2), in which the content of either silicon or oxygen is changed. These oxides are no longer SiO_2 and have to be represented by SiO_X where x is between zero and two. When x is equal 2, the dielectric is SiO_2; whereas when x is zero, then it is amorphous or poly crystal line silicon. For any value of x between 0 and 2, the dielectric is non-stoichiometric silicon oxide. Silicon rich oxide (SRO) presents small silicon islands embedded in silicon dioxide matrix. This circumstance drastically changes its electric property with respect to silicon dioxide.

SRO can be deposited by low-pressure chemical vapour deposition (LPCVD) in an evacuated furnace through which there is a flow of silane (SiH_4) and nitrous oxide (N_20). The excess silicon can be judged by the ratio of these gases $R_0 = N_2O/SiH_4$.

In the SRO, electrons can move between the silicon islands by tunneling [1]. Thus, the SRO layer at certain value of R_0 is likewise to a leaky insulator that exhibits considerable steady state current flow even at relatively small electric field applied. If such SRO layer is sandwiched between a metallic electrode and a semiconductor (metal-insulator-semiconductor (MIS) structure), new physical effects can be achieved. It has been shown [2] that the d. c. current through the insulator introduces deviation of this structure from a standard MOS capacitor. The application of a substrate-depleting d. c. voltage establishes a steady-state non-equilibrium depletion regime [2,3]. This regime is characterized by an equality of the minority current generated (in the bulk of the substrate and at the interface with the insulator) and the thorough current across the insulator to a metallic gate. The current depends on the voltage drop across the leaky insulator and the excess surface minority carriers density because of the charge accumulated in the space charge region. Any change in the generation current will produce new current equality and a new value of the charge in the space charge region. If the majority-carrier current through the insulator is small and the bias voltage is sufficient to maintain the steady-state non-equilibrium depletion regime, the electrical characteristics of such structure are likewise to those of an abrupt p-n junction. M. Aceves et al [4] investigated the AI/SRO/Si under this mode of operation, for the first time. However, opacity of Al contact was a limitation to obtain the real value of photocurrent. Quantitative assessment of the photocurrent in a steady-state non-equilibrium mode was

done in [5], when Al non-transparent contact was replaced by conducting transparent fluorine-doped tin oxide layer.

At lower bias, the transport of generated minority carriers through the insulator is limited, and a stable inversion layer will form at the semiconductor surface. At this bias, the structure will operate in an equilibrium MOS capacitor mode. A rapid increase of the voltage bias can disturb this equilibrium state. Then, the sensor goes in a non-equilibrium state due to the increase of the potential well capacity at the SRO/silicon interface. The initial quasi-equilibrium state will be reached only when through some time the potential well is tilled by thermal or photogenerated minority carriers. This time is named stored time. Illumination will accelerate the storage process. Recently, we show, for the first time, that this process can be used in new optical sensors with essential internal gain [6]. The mechanism is not only characteristic of structures with SRO layer, but it can take place also in metal-insulator-semiconductor structures with SiO_2 Si_3N_4 and other types of insulator as a metal-phthalocyanine organic semiconductor [7], for example. Based on this principle the conception of new optical sensors has been formulated [8]. Accordingly this conception photo-induced charge inside the semiconductor substrate can be stored in the potential well at insulator/silicon interface. Increasing the gate voltage that switches the structure in deep depletion mode forms this potential well. Then, the stored charge can be readout by retaining the gate voltage bias to the initial value after time called the integration time, which is smaller then the stored time. At that, a displacement current peak with amplitude much more then photocurrent takes place in the circuit. At fixed integration time, the amplitude of this current peak is proportional to the light intensity and essential internal amplification of the electrical signal is obtained. Proposed sensors can be used for a weak optical signal registration. Moreover, because the sensor works in integration mode, it is useful also for registration of modulated optical signals. In this application the modulation frequency is not important since the collection time of the minority photo generated carriers is determined by the electric field in the depletion region and this time is much less than the integration time.

The goal of this article is to present additional new experimental results of the FTO/SRO/Si structures, to better understand photo detectors based on MIS capacitor.

II. Experimental details

A. Samples Fabrication

The FTO/SRO/Si sensors were prepared by depositing SRO layer on high-resistive n-type silicon substrate with carrier concentration about of 10^{12} cm^{-3}. The SRO with silicon excess of 8.5 at. % was deposited in a hot-wall LPCVD reactor. Silane, diluted to 5% in nitrogen, and nitrous oxide were used as reactants with an $R_0 = 20$. Samples were sintered in a nitrogen ambient at $T = 1000^0C$ for 30 minutes after deposition of SRO. The thickness of the SRO layer was determined both by ellipsometry with a Gartner 117 ellipsometer and by profilling with a Tencor Surface Profilometer Alphastep 200. In both cases, the average of the measurement was taken as the thickness of the SRO film, Transparent conducting n-type fluorine-doped tin oxide (FTO) layer as the gate electrode was deposited on the surface of SRO by spray technique [9]. The conduction properties of FTO film are similar to that of a metallic layer due to its big carrier concentration (~ $10^{20}cm^{-3}$). Moreover, high transparency of FTO in visible and near infrared spectral range (more than 80 %) allows an effective light penetration inside the silicon substrate. HTO film was subsequently etched to a rectangular shape of $6x10^{-2}$ cm^2.

B. Measurement Details

Dynamic current-voltage (I-V) and capacitance-voltage (C-V) characteristics were obtained by a linear ramp voltage method with a Wavetek pulse/function generator. Characteristics were recorded with a Tektronix TDS-3012 digital oscilloscope equipped with a Tektronix ADA4GOA preamplifier. The investigated structures were connected in serial with a function generator and a load resistor.

At a linear voltage sweep $U(t) = Uo \pm \alpha t$, the output signal is proportional to the capacity of the structure:

$$U_{out}(t) = -R_L C\left|dU(t)/dt\right|,$$

where C is the capacitance of FTO/SRO/Si sensor and R_L is a load resistor ($R_L = 50$ kΩ), The output signal is

$$U_{out} = \left|\alpha R_L C(t)\right| \text{ or } I(t) = \left|\alpha C(t)\right|. \quad (1)$$

Thus, using the linear ramp voltage method, it is possible to obtain the C-V characteristic of MOS capacitors at low and intermediate sweep rates.

The transient processes were studied using a trapezoidal voltage together with a constant voltage bias (DC offset) with a Wavetek generator.

A monochromator or light-emitting diode (LED) was used to carry out the photoelectric measurements.

III. Experimental results

A. Characteristics with a linear voltage sweep

Dynamic (I-V) characteristics (Fig. 1) of fabricated MOS capacitors have been recorded when a triangular voltage with intermediate sweep rate was applied to the FTQ gate of the capacitor. At that, the structure capacity is proportional to the recorded displacement current. Consider the first part of I-V characteristic when $dU/dt < 0$. Judging from the first picture in Fig. 1, one can make the solution that the sweep rate of 2.2 V/s is too slow for minority carriers to follow the gate bias sweep and to form an inversion layer. Formation of such layer is seen clearly at – 7 V bias on the first picture in Fig. 1. At that, displacement current behavior is the same in dark and under illumination. However, how it will be shown below, the minority carrier response time in strong inversion is about 1.2 sec. Because this response time is very long, the sweeping rate 2.2 V/s is too fast for

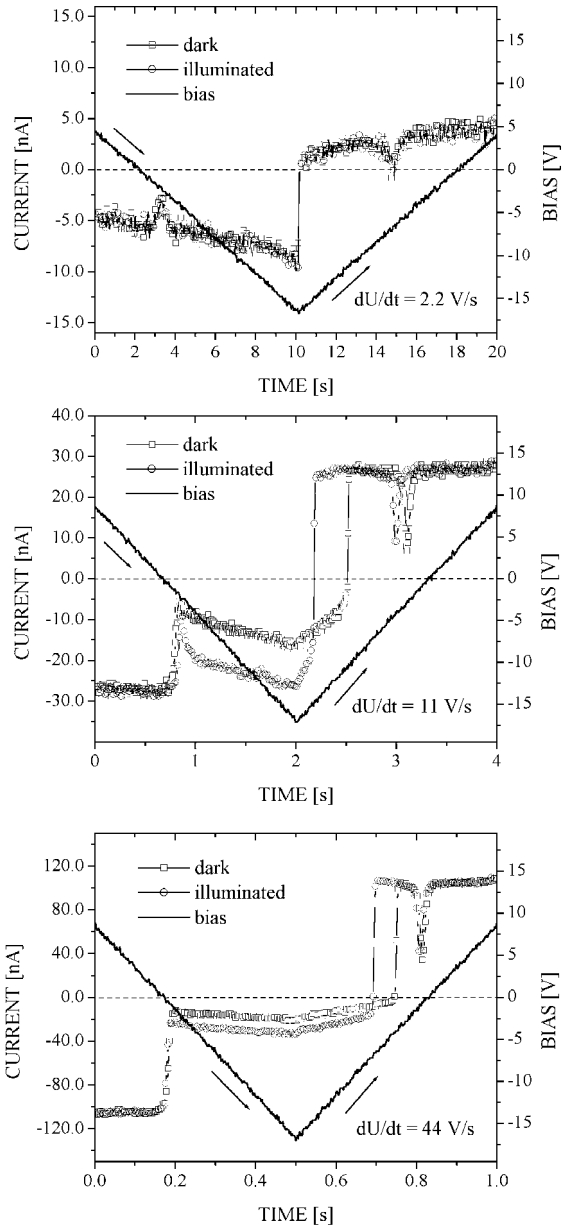

Fig. 1. Dynamic I-V characteristics of fabricated MOS capacitor recorded when a triangular sweep voltage at different sweep rates was applied to the FTO gate.

minority carriers to follow the gate bias sweep. Consequently, as gate bias sweeps into inversion, no strong inversion layer forms.

Our experiment shows that SRO negative charge beyond the gate is responsible for appearance of obtained pseudo-inversion at dU/dt = 2.2 V/s. This charge does not affect the capacitance in accumulation and depletion. However, when oxide charge beyond the gate inverts the surface, a weak inversion layer that is formed under the FTO gate has connection with this surface inverted layer and the measured capacitance rises to the capacity of the SRO layer. Illumination docs not affect on the capacitance behaviour.

At bigger dU/dt (11 V/s and 44 V/s) and dark condition the formation of weak inversion layer, which then has a contact with surface inverted layer, requires more time. Thus, this process takes place during some time interval when the sign of dU/dt is changed. Illumination decreases the minority carrier response time and accelerates this process. At the return sweep (dU/dt > 0), the structure moves towards the accumulation state because the band bending at the silicon surface under FTO gate decreases. At the same minority carrier generation rate and at certain voltage bias, decreasing the surface potential in silicon assists the formation of weak inversion layer under the gate. This layer immediately connects with surface inverted layer beyond the gate and, as a result, the structure rapidly switches to strong inversion mode where the capacitance is determined by SRO parameters. Sample illumination accelerates the format ion of weak inversion layer under the gate due to increased minority carrier generation rate. At that, the transition to above mentioned inversion mode requires smaller bias changes. Further decreasing the bias causes the depletion and the accumulation modes of the capacitor that is shown in upper parts of Fig. 1.

The question about a pseudo-inversion layer formation was investigated separately in semitransparent metal-silicon dioxide-silicon (MOS) structures fabricated in the same n-type material Our experimental conditions allow us to fabricate the MOS structure where silicon dioxide thermal grown layer has either positive (that is usual for thermally grown oxide) or negative charge. The last was prepared a special chemical and thermal treatment the MOS structure with initially positive charge in SiO_2 layer. Fig. 2 shows the dynamic I-V

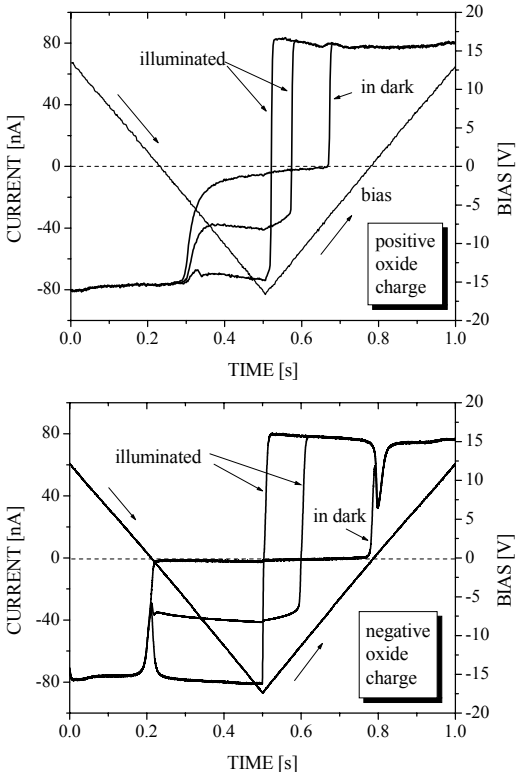

Fig. 2. Dynamic I-V characteristics of fabricated MOS capacitor with silicon dioxide as insulator with positive (above) and negative (below) charge recorded when a triangular sweep voltage (60 V/s) was applied to the gate.

characteristics of these MOS structures when linear voltage sweep (60 V/s) was applied to the metallic semitransparent gate.

Negative charge in SiO_2 causes the appearance of surface inverted layer at silicon interface beyond the gate. At that, a pseudo-inversion arises in MOS capacitor I-V characteristic with the same formation mechanism as was described in FTO/SRO/Si structures, structure in strong inversion mode. After that, the structure is likewise a capacitor and a displacement photocurrent current, has a differential shape.

Fig. 3 shows I-V characteristics of the FTO/SRO/Si structure in the dark (a) and illumination (b) recorded when linear voltage sweep bias from – 20 V to 0.5 V with dU/dt = 400 V/s was applied to the gate.

The value of the current in Fig. 3b was recalculated using equation (1) to obtain the C-V characteristic (insertion in Fig. 3b). From this, the thickness of the SRO layer is determined as 0.16 μm that agrees with the measured thickness obtained by ellipsometric and profilometric methods.

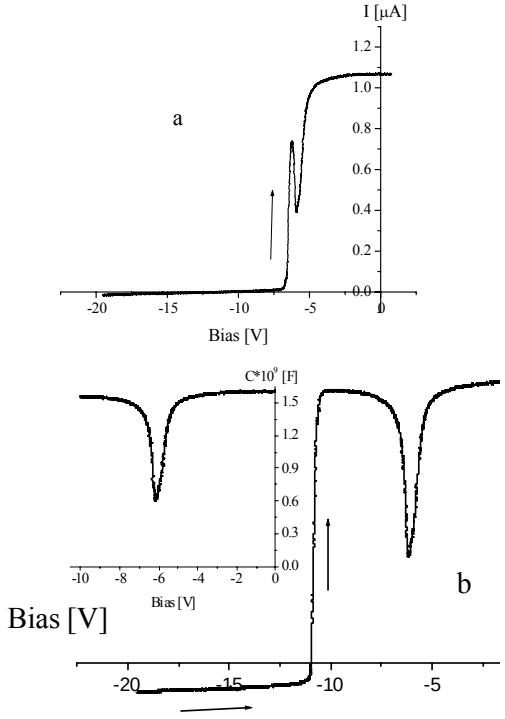

Fig. 3. Dynamic I-V characteristics recorded when linear sweep bias from –20 V to 0.5 V with dU/dt = 400 V/s was applied to the FTO/SRO/Si sensor: a - m the dark; b - at illumination.

Fig. 4 shows illuminated dynamic I-V characteristics in one of fabricated sensor when linear sweep voltage was applied to the gate. This sample was illuminated using a square-wave modulated LED emission. In non-equilibrium depletion-operating mode photogenerated holes try to restore the equilibrium disturbed by applying the gate sweep voltage with dU/dt < 0. As a result,

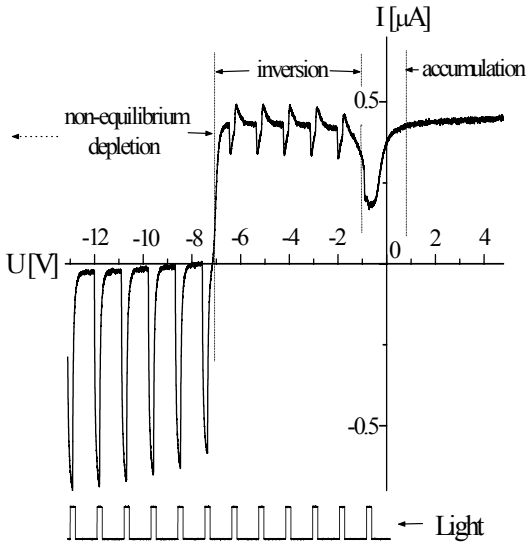

Fig. 4. The I-V characteristic of FTO/SRO/Si structure recorded at linear sweep bias and a square-wave modulated light with wavelength of 930 nm.

minority carrier photocurrent takes place. At that, the operational mode of the structure is likewise an usual p-n photodiode. The output current reproduces the modulated light shape. The photogenerated holes are driven to SRO/Si interface to fill the potential well formed by a negative voltage bias applied to the SRO electrode. However, sweeping gate bias into inversion is too fast for minority carriers to follow it and to form a strong inversion layer. At dU/dt > 0, decreasing the voltage bias reduces the band bending at the silicon interface and at - 7 V a weak inversion layer under the gate connects electrically with inversion surface layer beyond the gate causing transition of the structure in strong inversion mode. After that, the structure is likewise a capacitor and a displacement photocurrent current has a differential shape.

Depending on the illumination level, transition into strong inversion mode takes place at different voltage bias or voltage threshold (Fig. 5). The curve 1 was taken

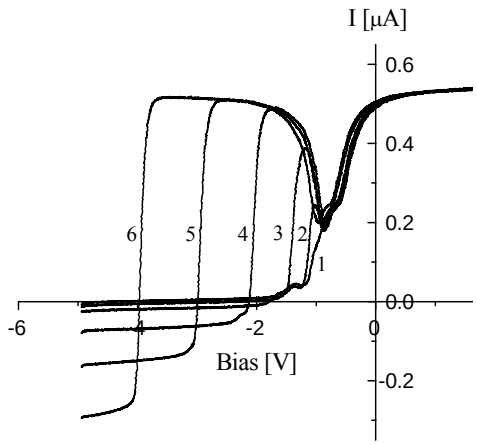

Fig. 5. The I-V characteristic of FTO/SRO/Si sensor recorded at a linear sweep bias and at different illumination levels, from dark (1) to maximum illumination (6).

in dark, and curves 2 to 6 were taken under increasing illumination level.

IV. Photo electric characteristics in non-equilibrium mode

This type of operation is obtained under two conditions. The first is that a constant voltage applied to the structure causes an initial inversion under the gate. This voltage can be very low, close to zero, if SRO layer is negatively charged. The second one is to put on a trapezoidal depleting voltage pulse in addition to a constant voltage bias. This pulse causes transition of the structure in a non-equilibrium mode. If the voltage pulse is long, generated minority carriers try to restore the equilibrium. This process is accompanied by a displacement current in the circuit.

The displacement current versus time (in dark and under illumination) when a long trapezoidal pulse is applied to the structure is shown in Fig. 6. Pulse voltage bias is added to a constant bias, at which the structure is in the first quasi-equilibrium inversion mode. Results in Fig. 6 show that displacement current decreases in time. It is because thermal or photo generated holes fill up the potential well created by a pulse bias. Displacement current is zero, when the potential well at the SRO/Si interface is filled completely. At dark conditions, this time (the storage time) is about 1.2 seconds. A monochromatic backlighting decreases the storage time. When the potential well is full, the structure goes into the second quasi-equilibrium inversion state with a bigger inversion charge.

Readout procedure to have the information about stored charge takes place if the structure is returned into the initial inversion state by rapid decreasing the voltage bias to the initial constant value. The stored charge (holes), at that, injects into silicon. These excess holes recombine with electrons inside the silicon substrate. As result, a displacement current peak (3.4 μA) appears at trailing edge of a trapezoidal pulse.

Fig. 7 shows the displacement photocurrent in the FTO/SRO/Si MIS capacitor sensors, when the device is biased with a negative 10 V constant voltage and a 10 V trapezoidal voltage pulse is added to this constant voltage. The integration lime (the duration of a trapezoidal pulse) is 100 ms and it is smaller than the storage time in dark (1.2 s). Illumination was provided with a 930 nm LED. It is easy to see that the amplitude of the readout current peak (about 80 μA) is 700 times bigger than the 80 nA photocurrent that flows to charge the FTO/SRO/Si capacitor.

The reason of this is the ratio of charging and recharging times (100 ms and 0.004 ms, respectively) taken into account that the stored charge in the potential well during the integration time and the charge injected into the substrate is nearly the same.

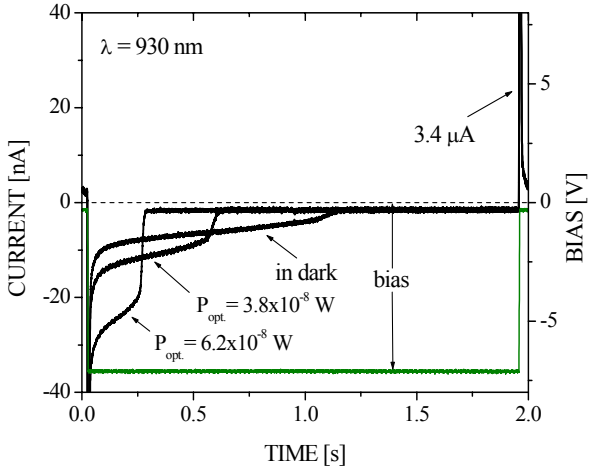

Fig. 6. Displacement current vs time (in dark and under illumination), when a long trapezoidal pulse (- 7 V) is applied to the structure in addition - 0.3 V constant bias.

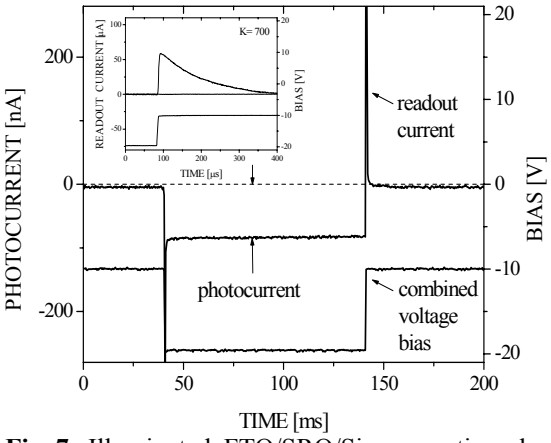

Fig. 7. Illuminated FTO/SRO/Si sensor time-depended current characteristics at two-level stepwise voltage bias applied to the structure. Combined voltage bias is a superposition of a 10 V constant voltage and 10 V trapezoidal voltage pulse. Inset shows the readout current peak at trailing edge of the trapezoidal voltage pulses.

Thus, the current gain in this case is 700. In other words, the investigated sensors have essential internal amplification of the electrical signal, then they can be used to sense weak optical signals. Moreover, our experiment shows that these sensors can be used also to register weak modulated optical signals. Moreover, the modulation frequency of the optical signal is not important due to the integration of photogenerated charge that has not the dependence from RC constant that is important in design of high-speed *p-i-n* photodetectors. This fact opens the possibility to use large-area MIS capacitor sensors also as sensitive detectors of high-frequency modulated optical signals.

The transient processes in the structures under investigations have been simulated by means of a circuit model (see details in [10]). The basic equations are the second Kirchhoff's law for the circuit and the equation for the charge of MOS capacitor. A full depletion approximation is used for depleted layer within n^- Si. The charge sources at the integration stage include volume

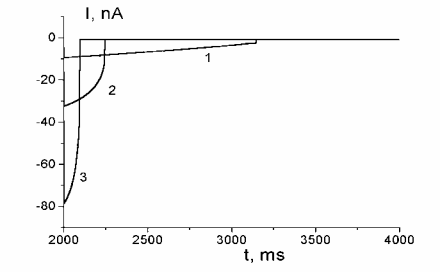

Fig. 8. Simulated dependencies of electric current on time for integration. A transient U = -10 V to U = -20 V takes place at the time moment t = 2000 ms. Curve 1 is at dark, curve 2 is for the carrier generation rate for the unit of volume $G_0 = 10^{15}$ cm^{-3}s^{-1}, curve 3 is for $G_0 = 3\text{x}10^{15}$ cm^{-3}s^{-1}.

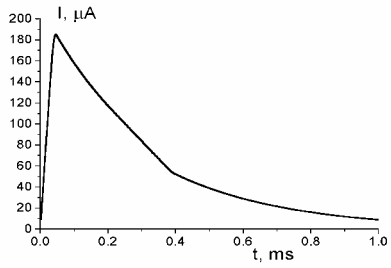

Fig. 9. Simulated dependencies of electric current on time for readout. A duration of the transient from U = -20 V to U = -10 V is 6 μs.

thermo generation and photo generation. The following parameters have been used: the depth of Si-rich oxide is 0.16 μm, the transverse area is $A = 3\text{x}10^{-2}$ cm^2, a dielectric permittivity is $\varepsilon \approx 4$. The generation time in n$^-$ Si is used as τ_g = 66 μs and lifetime for holes is τ_p = 3.6 μs. Under these values of generation time and lifetime, a coincidence of simulations and measurements of storage time takes place. The load resistor is R_L = 50 KΩ. A duration of transients of voltage from U = -20 V to U= -10 V (for readout) is 6 μs. A value of leakage current is about 0.6 nA for U = -20V (see Fig. 8). Typical results of simulations are given in Fig. 8 for integration and in Fig. 9 for readout. In the Fig. 8, dependencies of the current within the circuit on time are presented at the dark (curve 1, $G_0 = 0$) and for different levels of illumination (curve 2, $G_0 = 10^{15}$ cm^{-3}s^{-1}, curve 3, $G_0 = 3\text{x}10^{15}$ cm^{-3}s^{-1}). Here $G_0 = \alpha J_0/(h\nu)$ is a carrier generation rate per unit volume by infra red radiation of the input intensity J_0; α = 200 cm^{-1} is a dissipation coefficient for infrared radiation at λ_0 = 930 nm. One can see that a maximal value of the current under readout is about $2\text{x}10^4$ times greater than one under integration in the dark. At illumination, a ratio of readout and integration currents is $10^3 - 10^4$.

V. Conclusion

The experimental results of investigations MIS structures on a base of Si-rich oxide demonstrated a possibility for using these structures as optical sensors with internal signal amplification. Numerical simulations qualitatively confirm experimental results.

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Застосуваня збагачених оксидами кремнієвих плівок в новітніх оптоелектронних приладах

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Описані оптоелектронні властивості нових оптичних датчиків метал-ізолятор-кремній (МІК). Шар збагачений оксидом кремнію використовується як ізолятор. Ми обговорюємо випадок, коли напруга зміщення не є достатньою для струму, що протікає через шар кремнію збагаченого оксидом. Датчик представляє конденсатор МІК, фотоелектричні властивості якого досліджені і чисельно описані. Це вказує на те, що ступенева напруга зміщення датчика діє в двох квазі-рівноважних методах. Перехід між цими методами представляє практичний інтерес. В першому операційній моді, фотогенеровані неосновні носії зберігаються в потенціалі кремнію збагаченому оксидом на поверхні розділу. Збереження заряду відбувається при зміні, що наступає через застосовувану напруга зміщення. Тому інверсний заряд інжектується в кремнієву підкладку і спостерігається пік зсуву по струму. Амплітуда цього піку перевищує надмірне значення фотоструму в стадії збереження. Внутрішній коефіцієнт розширення струму перевищує значення 10^4. Тому, досліджувані датчики мають внутрішнє розширення електричного сигналу і вони можуть використовуватися для слабкої оптичної сигнальної реєстрації. Чисельна модель вказує на присутність інверсію і областей збіднення в напівпровіднику, а також враховує витік через збагачений оксидом кремній. Проведено моделювання для експериментальних вхідних параметрів і показано добре узгодження з експериментальними результатами.