ФІЗИКА І ХІМІЯ ТВЕРДОГО ТІЛА
Т. 4, № 3 (2003) с. 491-497

PHYSICS AND CHEMISTRY OF SOLID STATE
V. 4, № 3 (2003) p. 491-497

PACS 85.30-KK; 61.50-AH

ISSN 1729-4428

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Modeling of physical properties and experimental results for virtual p-i-n diode based on metal-insulator-silicon structure

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A study of the physical processes in metal-insulator-semiconductor (MIS) capacitors gives a new way of using this familiar device as a high-sensitive optical sensor with giant internal amplification of an input signal. New CMOS optical sensors with a metal – insulator – semiconductor structure are developed and investigated both theoretically and experimentally. The physical properties of these sensors are described with a model of MIS capacitor where a presence of depletion layer of electrons, an inversion layer of holes of a finite depth, and possible change of properties of n- semiconductor layer are taken into account. Two-level voltage bias provides a transient between two quasi-equilibrium inversion modes. This transient is applied both for storage and for readout of the input optical signal for quantitative measurements of a weak infra red radiation. Proposed simple readout procedure provides reading the integrated information with a significant amplification. At the readout stage, a resistance of the n-semiconductor layer changes drastically, and the MIS structure behaves as a virtual p-i-n - diode with double injection of carriers into the n- layer. An amplification (or the current transformation coefficient) is determined by the ratio of integration and readout times and it is about 104 – 105 at great external loads (>10 KΩ) and reaches the value of 106 at small loads (~100 Ω). A theoretical model explains a behavior of the sensor under storage by thermo generated carriers and by photo generated ones jointly. Numerical simulations are of a good agreement with experimental investigations of proposed sensors.

Keywords: diode, metal-insulator-silicon structure, sensors.

Стаття поступила до редакції 19.05.2006; прийнята до друку 23.08.2003.

I. Introduction

Invention of a charge-coupled device (CCD) and a charge-injection device (CID) [1] was a revolutionary step in the history of electronics imagers. As since the basic physical properties of a CCD or CID were known before their invention, these devices are not new devices. However, by the way their developing, a new approach of using an old and familiar device, i. e. a metal-insulator-semiconductor (MIS) capacitor has been shown, and new ideas in circuits and signal-handling systems have been realized. The first basic operating principle of CCD and CID is very simple. If a voltage bias is applied to a MIS capacitor, then the underlying semiconductor is depleted of majority carriers and photon-generated minority carriers can be collected and stored in a surface inversion region. A possibility to locally integrate photogenerated carriers into a charge packet over a certain amount time allows to overlap the main limitation of an usual p-n based photodetectors: impossibility to transport a single electron or hole to an output stage and to convert it to a measurable quantity. In CCD and CID all sensing single MIS capacitors are coupled together and the optimization of both transferring and readout modes are quite important to possess an image quality. This is why, for instance, a more simple readout method by a direct injection of stored charge in substrate has not found an application in arrays based on CCD or CID [2].

However, some essential limitations taking place in CCD and CID are not important for the single MIS capacitor operated in the CID sensor mode. At that, two circumstances are essential in the case of applying the single MIS capacitor for a radiation sensing:

- such a photodetector can operate with very high interface state densities [2];
- to obtain the information about the stored signal charge, the most simple direct injection readout method [2] can be applied without the limitation that is proper for CCD and CID.

Hence, these circumstances allow designing the extremely simple MIS capacitor-based integrating photodetector, the main destination of which is to record weak radiation intensities. The first attempt to use CCD (or CID) principles in a single photodetector was reported in [3-6], where a charge-accumulation-and-multiplication photodetector was developed. This detector contains three coupled MIS capacitors designed as photodetector, transfer, and avalanche gates. The photo current at the detector gate is first integrated with the transfer gate closed and with the avalanche gate ramping toward avalanche voltage. Integrated charge is then transferred to the avalanche gate where charge multiplication occurs. That process induces a displacement current pulse for readout, which is proportional to the photo current, the integration time, and the multiplication gain factor, and is inversely proportional to the transfer time. Such cooled photo detector is suitable for detecting photons of extremely low fluxes with an internal amplification, however, the design of it and the measurement circuit are complicated. But, non-steady physical processes in MIS structures are not investigated properly yet.

Thus, the aim of this work is:

- to investigate non-steady processes in MIS structures used practically in CCD and CID based devices;
- through a profound study of time-dependent physical processes in the single metal-insulator-semiconductor (MIS) capacitor operated in both the storage and the readout CID modes and connected in a simple measuring circuit to make a numerical modeling of this device;
- to show an applicability of the most simple charge injection readout mode to obtain the output signal with a giant internal amplification.

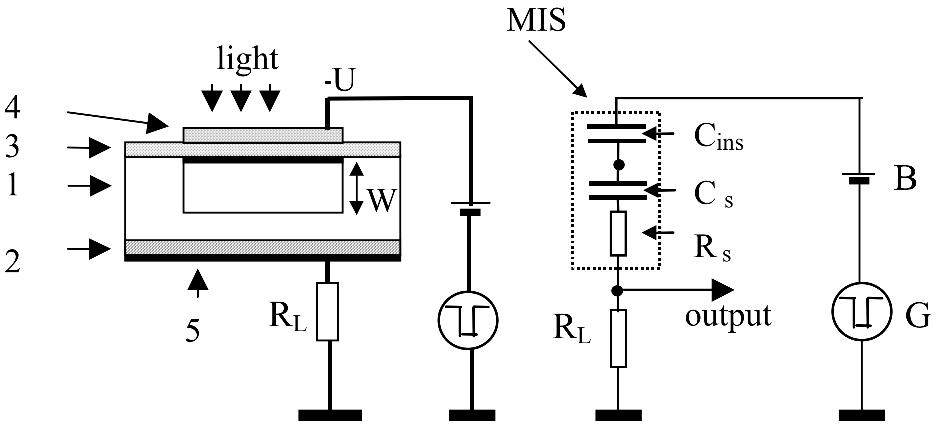
II. Model of the Device and Numerical Simulations

The MIS capacitor structure is shown in a Figure 1 a. One plate of the capacitor is the high resistive n-type silicon layer (1) whose resistivity corresponding to a doping of $N_D \approx 10^{12}$ cm^{-3}. Implanted n^+ layer (2) is on the backside of the silicon layer to create an ohmic junction with a metallic layer (5). The insulating layer (3) is SiO_2 or SiO_2/Si_3N_4. The gate (4) is semitransparent metallic layer.

Due to that the oxide capacitance (C_{ins}) and depleted silicon capacitance (C_b) are connected in series (see Figure 1 b), the capacitance of the MIS structure depends on the voltage (bias) on the gate. A voltage is applied to the gate while the backside of the semiconductor is grounded. For the purposes of this work, we shall consider that applied negative voltage U is significantly larger by its absolute value that threshold voltage (U_{th}), which demarcates the depletion regime from the inversion one. Thus, at any applied voltage from a battery (B) the semiconductor surface is inverted because carriers of the opposite type from the semiconductor layer accumulate at the silicon surface.

A Figure 2 shows a dependence of the inversion charge $Q_p = - C_{ox}(U-U_{th})$ as a function of the applied voltage in a quasi-static situation. At U_1 the inversion charge is Q_{p1} (point A in the Figure 2) and the structure is in the equilibrium inversion state. If in time moment t_0 the voltage changes rapidly to a bigger value U_2 (transition from A to B), the capacity of the potential well at insulator/silicon interface increases because repulsion of the majority carriers only takes a time scale of the dielectric time constant.

The width W(t) of depletion layer will expand beyond the value of the depletion width at the stationary inversion state, and the structure is now in the non-equilibrium state. If U_2 is held constant, then the charge distribution will revert back to the equilibrium situation (transition from B to C) with the equilibrium Q_{p2} value and W snaps back to the value determined by the inversion conditions. This process causes the displacement current flow in the silicon substrate. Thus, the charge storage takes place during the time interval t_o-t_1. The storage time that is necessary to fill the potential well at U_2 is a few orders bigger than the generation time of the minority carriers in the depletion region. If the applied voltage is changed rapidly from U_2 to U_1 (transition from C to A), the inversion charge $\Delta Q_p \approx -C_{ox}[U_2-U_1]$ will be injected into the silicon substrate and the displacement current peak in the circuit



a b

Fig. 1. The MIS capacitor structure (a) and measuring circuit (b). The MIS capacitor equivalent is shown in dotted frame. R_s and R_L are the resistances of the undepleted silicon bulk and load resistor, respectively.

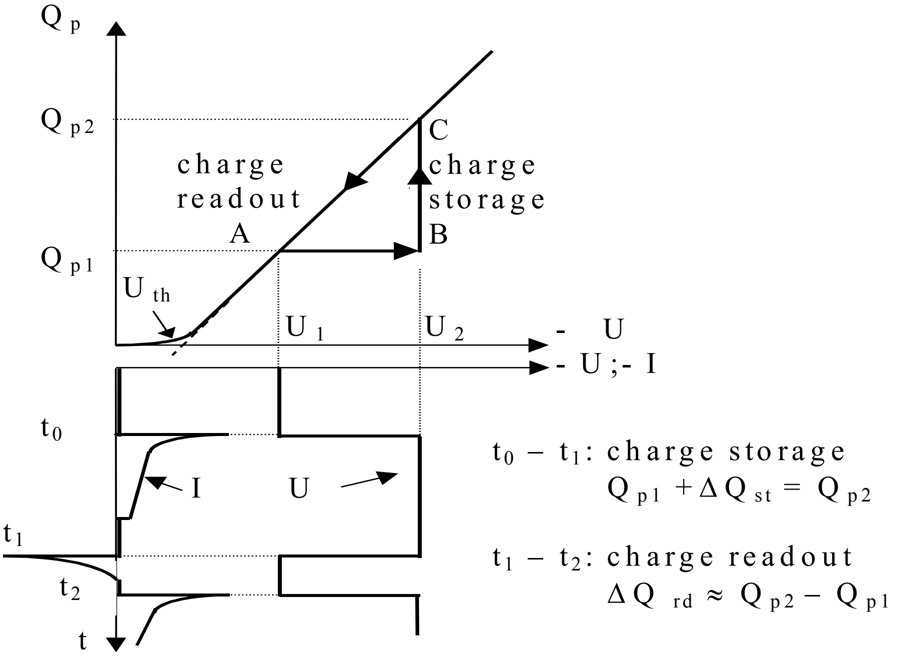


Fig. 2. The inversion charge density as a function of the applied voltage (upper figure). Lower figure shows time-dependent voltage bias and a displacement current in circuit (Figure 1b).

can be obtained. This is readout mode to see the stored charge.

It has been found experimentally that the amplitude of the readout current is significantly (many orders) bigger than the value of the storing current. This fact allows us to design new photo detectors with giant internal amplification of the signal. To understand the device operating parameters, numerical calculations have been done based on a model presented here.

A description of a transient behavior of the MIS structure under investigations can be carried out within a framework of a circuit model. The electric circuit and equivalent electric measuring circuit have been shown in the Fig. 1. Transients in MIS structures were investigated theoretically in some works [1]. But a behavior of MIS structure was considered separately there, when ignoring the external electric circuit.

The applied voltage U(t) is step-like (see the Fig. 2):

$$U(t)=\begin{cases}-|U_1|\equiv -10\ \text{V};\ t<t_0;\\ -|U_2|\equiv -20\ \text{V},\ t_0<t<t_1;\\ -|U_2|-(|U_1|-|U_2|)\dfrac{t-t_1}{\Delta T},\ t_1<t<t_1+\Delta T;\\ -|U_1|,\ t_1+\Delta T<t<t_2.\end{cases} \tag{1}$$

Thus, since $t = t_0$ till $t = t_1$, a storage takes place; at $t > t_1$, a readout occurs (see the Fig. 2). Parameter ΔT determines the duration of a transition of the applied voltage under readout from $-|U_2|$ to $-|U_1|$. It is about 1 μs in the experiments.

Integration process is charging the MIS capacitor due to thermo- and photo generated carriers. An influence of external circuit is not essential there, because of small charging current (< 1 μA). In dark, observed values of the integration current were about 1 – 5 nA. Below, an attention is given to readout (discharge), because namely under the discharge the properties of external circuit affect essentially the dynamics of process. The basic equation is the second Kirchhoff's rule for the total electric circuit:

$$\begin{aligned}&-U(t)=\frac{Q}{C_{ins}}-I(R_L+R_s);\\ &I(t)=-\frac{dQ}{dt};\\ &R_s(t)=\frac{1}{qA}\int_0^{d_n}\frac{dz}{\mu_p p(z,t)-\mu_n n(z,t)};\end{aligned} \tag{2}$$

The Eq.(2) is valid, when the discharge stars from the fully filled potential well (inversion layer of holes). Here Q is the total charge of the MIS capacitor, $Q \approx Q_p$ for fully filled potential well, Q_p is the charge of holes within the inversion layer. I(t) the electric current in the circuit, R_L, R_s are the resistances of external load and n^- Si, respectively; $C_{ins} = \varepsilon_0\varepsilon_i A/d_i$ is a capacitance of MIS capacitor, A is a transverse area of MIS capacitor, d_i is the depth of dielectric, $\varepsilon_i = 3.9$ is its dielectric permittivity (SiO_2). In our simulations, the values are $A = 0.0314$ cm^2, $d_i = 0.07$ μm, The resistance of n^- Si is expressed through concentrations of electrons and holes n, p, their mobilities μ_n, μ_p, and the depth of n^- Si layer $d_n = 700$ μm. Because duration of readout stage is short (about 1 ms and smaller), it is possible to neglect by an influence of thermo and photo generation there. Also, it is possible to neglect by an influence of the voltage drop at the inversion layer U_p at the readout stage. But the voltage drops at the external load $I \cdot R_L$ and at the n^- layer of semiconductor $I \cdot R_s$ are dominating there.

At the readout stage, a quick discharge of MIS capacitor takes place. The simulations of readout process have been done for a duration ΔT of a voltage drop from $-|U_2|$ to $-|U_1|$ equal to $\Delta T = 1$ μs. During the readout, the holes from an inversion layer move into n^- semiconductor layer. Simultaneously, an injection of electrons from n^+-n^- semiconductor junction takes place, too. Therefore, a double injection of carriers into n^- layer takes place and its resistance changes drastically. Thus, under the readout stage, MIS structure behaves as a 'virtual' p-i-n diode with a double injection of carriers. An influence of variable resistance of n^- layer on discharge depends on the value of external load. At large values of $R_L > 10$ kΩ, this influence is unessential, because the biggest value of the resistance of n^- layer is ~ 8 kΩ. But, under smaller values of the external load, this influence is dominating. Thus, it is necessary to consider readout process under various values of external load R_L.

To simulate discharge process, it is necessary to solve the Eq.(2) jointly with diffusion-drift equations for concentrations of carriers and Poisson equation for electric potential within n^- layer [7,8]:

$$\frac{\partial p}{\partial t} + D_p \frac{\partial}{\partial z}\left(\frac{1}{U_T} pE - \frac{\partial p}{\partial z}\right) = -\frac{pn}{(p+n)\tau_{p0}}; \qquad \frac{\partial n}{\partial t} - D_n \frac{\partial}{\partial z}\left(\frac{1}{U_T} nE + \frac{\partial n}{\partial z}\right) = -\frac{pn}{(p+n)\tau_{p0}};$$
$$\frac{\partial^2 \varphi}{\partial z^2} = -\frac{q}{\varepsilon_0 \varepsilon_s}(p - n + N_D); \qquad (3)$$

Here p(z,t), n(z,t) are concentrations of electrons and holes, φ(z,t) is electric potential, $E = -\partial\varphi/\partial z$ is electric field, $D_{p,n}$ are diffusion coefficients; $U_T = k_B T/q = 0.025$ V. The simplest form of recombination term has been used with only one lifetime $\tau_{p0} = \tau_{n0}$.

The boundary conditions for concentrations and the electric potential are:

$$D_p\left(\frac{1}{U_T} pE - \frac{\partial p}{\partial z}\right)\Big|_{z=0} = \frac{I}{qA}; D_n\left(\frac{1}{U_T} nE + \frac{\partial n}{\partial z}\right)\Big|_{z=0} = 0;$$
$$D_p\left(\frac{1}{U_T} pE - \frac{\partial p}{\partial z}\right)\Big|_{z=d_n} = 0; D_n\left(\frac{1}{U_T} nE + \frac{\partial n}{\partial z}\right)\Big|_{z=d_n} = \frac{I}{qA}; \quad (4)$$
$$\varphi\big|_{z=0} = IR_s; \quad \varphi\big|_{z=d_n} = 0.$$

Under readout, the left boundary may be considered as zero, because the width of inversion layer ($W \approx 10$ μm) is much smaller that the thickness of n^- layer $d_n = 700$ μm.

The initial conditions for concentrations are:

$$p(t=0,z) = p_0, \quad n(t=0,z) = N_D. \qquad (5)$$

The boundary conditions for concentrations express the fact that at the point z = 0 only injection of holes from inversion layer takes place, at the interface n^- - n^+ ($z = d_n$) only injection of electrons occurs. It is assumed that carriers within n^- layer are non-degenerated, so the Einstein relations for mobility and diffusion coefficients are valid. An influence of the voltage drop at the inversion layer U_p on the discharge dynamics is unessential there: $|U_p| < 0.5$ V. One can see that the problem is self-consistent, namely, the resistance of n^- layer is expressed through the concentrations of carriers; in that turn, the boundary conditions depend on the value of the electric current in the circuit I(t). When at the beginning of the discharge the potential well is completely full, the width of depletion region is $W \approx 0$ and total charge of MIS capacitor is equal to the charge of holes: $Q \approx Q_p$. If at the beginning of discharge the potential well is not full completely, then $dQ_p/dt = 0$ initially and the injection of holes into n^- layer is absent till the moment when depletion region disappears.

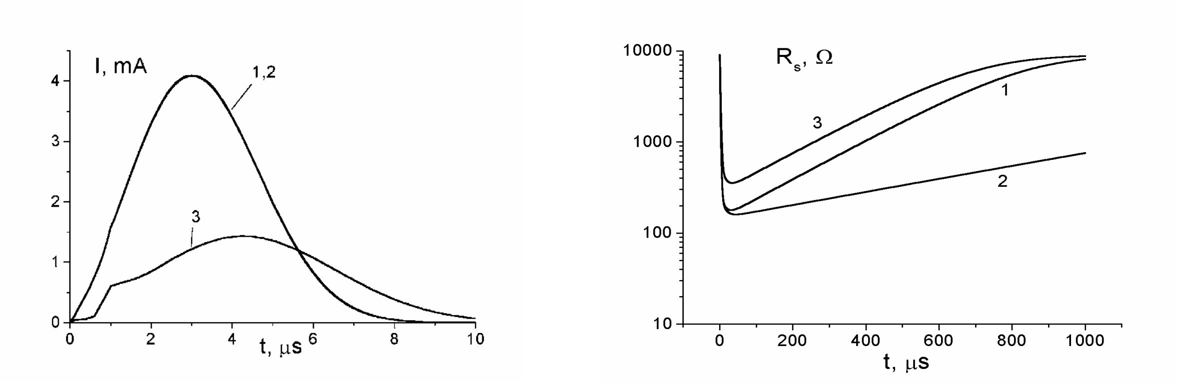
Diffusion-drift equations have been solved numerically by means of stable implicit difference scheme. Iterations have been used. Dependencies of readout current and of the resistance of n^- semiconductor layer are presented in Figs. 3, 4.

One sees that under discharge, resistance of n^- semiconductor layer (base of virtual p-i-n-diode) R_s is changed drastically, due to double injection of carriers. The initial value is about 8 kΩ and the minimal value may achieve 150 Ω. Thus, under smaller value of external load $R_L < 10$ kΩ, namely the resistance of n^- layer determines the dynamics of the current during discharge. Under greater values of $R_L > 10$ kΩ, changes of the resistance of the base do not influence the current in the total circuit.

In Figs. 3, 4, also dependencies for partially filled well also presented (curves 3). In this case, the total charge of MIS capacitor initially is due to both stored holes and the charge of donors within the depletion layer. Thus, primarily a decrease of the width of depletion layer W takes place, under unchanged value of the charge of holes Q_p. This leads to occurring some displacement current in the circuit. Then, the dynamics of discharge of Q_p can be described by the Eq.(2), under constant small value of $W \approx 10$ μm for $N_D = 10^{12}$ cm^{-3}, and $Q \approx Q_p$.

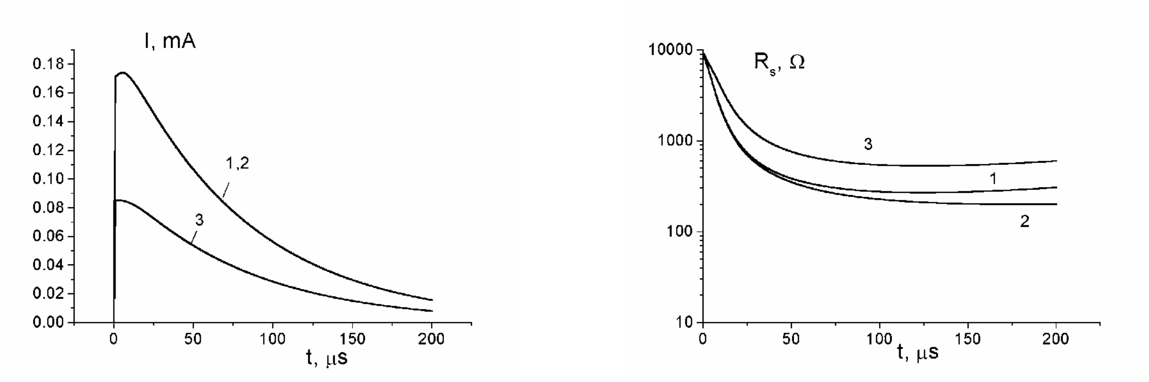
In a Fig. 5, spatial-temporal distributions of holes, injected from inversion region into n^- layer of semiconductor, are given. Initially, the distribution is non-uniform. Then, diffusion leads to almost uniform distribution. The time, which is necessary for total recombination of excess holes, is about $5\tau_{p0}$. Note also, that the minimal value of the resistance of n^- layer takes place with some delay with respect to the position of the maximum of the current.

Thus, using storing (integrating) the charge in MIS structure under irradiation by small intensities of infra



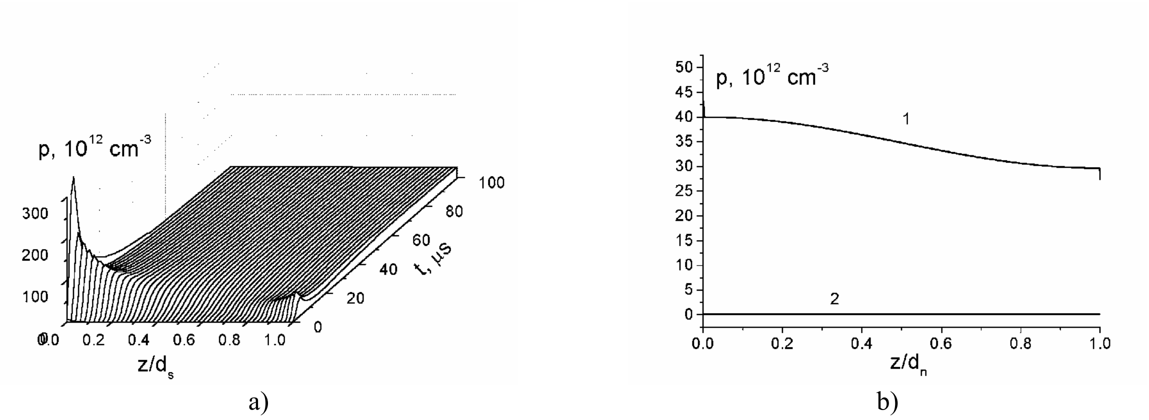
a) b)

Fig. 3. Dependencies of readout current (a) and the resistance of n$^-$ layer of semiconductor (b) on time for the load R_L = 50 Ω. Curve 1 is for lifetimes $\tau_{n0} = \tau_{p0}$ = 0.1 ms; curve 2 is for $\tau_{n0} = \tau_{p0}$ = 0.3 ms (the well is 100% full), curve 3 is for $\tau_{n0} = \tau_{p0}$ = 0.1 ms, but the well is 75% full.



a) b)

Fig. 4. Dependencies of readout current (a) and the resistance of n$^-$ layer of semiconductor (b) on time for the load R_L = 50 KΩ. Curve 1 is for $\tau_{n0} = \tau_{p0}$ = 0.1 ms; curve 2 is for $\tau_{n0} = \tau_{p0}$ = 0.3 ms (the well is 100% full), curve 3 is for $\tau_{n0} = \tau_{p0}$ = 0.1 ms, but the well is 75% full.



a) b)

Fig. 5. Distribution of concentration of holes within n$^-$ layer; a) is general spatial-temporal distribution, b) is for time moments t = 50 μs (curve 1) and t = 1000 μs (curve 2). The value of the load resistor is R_L = 50 Ω.

red light, it is possible to obtain essential values of the currents under readout. The ratio of peak values of readout currents and average values of writing currents may achieve 10^4 in the case of the values of the external load 10 – 50 KΩ and 10^6 when the external load is smaller than 1 KΩ, see the Fig. 3. The transition (switching) time of the applied voltage should be no bigger than the characteristic time of R-C circuit.

III. Conclusions

The theoretical and experimental investigations of the optical sensors based on a MIS structure have demonstrated an ability to record a weak radiation with a storage of an input infra red signal. Two-level negative voltage bias provides a transient between two quasi-equilibrium inversion modes. This transient is applied both for storage and for readout of the input optical signal for quantitative measurements of a weak infra red radiation. An influence of surface electronic states at the interface isolator – semiconductor on the charge storage is small, because the sensor works in the inversion modes only. Also, a value of a dark current due to thermo generation of carriers is quite small. Thus, an essential difference of storage and readout times may be achieved. The storage times may be about 0.1 – 10 s, but readout ones may be as small as 1 μs.

The ratio of storage and readout times determines a difference between average values of writing currents and peak values of readout ones. Writing currents are about 0.5 nA – 10 nA at a dark and under small values of infra red irradiation. The peak values of currents under readout may reach 1 mA and more. The internal current amplification (or the current transformation coefficient) is determined by the ratio of integration and readout times. It approximately is equal to the ratio of peak values of readout currents and average values of writing currents and may achieve 10^4 in the case of the values of the external load 10 – 50 KΩ and, when the external load is smaller than 1 KΩ, it may exceed 10^6. Thus, the sensors possess a giant internal current amplification. Under small external loads, smaller than 1 KΩ, a modulation of the resistance of the highly resistive silicon substrate by the carriers due to the double injection affects the temporal dynamics of the electric current essentially and the highly resistive substrate behaves as 'virtual' p-i-n- diode. A good agreement with the results of numerical simulations both of storage and readout with experimental results has been obtained.

Acknowledgement

The authors acknowledge the support of the Microelectronics Laboratory of INAOE in the preparation of the samples, especially W.A. Calleja, M. Landa, P. Alarcón, C. Zúniga and also A. Torres, A. Kosarev, J.DeLa Hidalga and D. Durini for an interest to this work and useful discussions.

This work was supported by CONACyT, Mexico Project 33812.

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О. Малік, В. Гримальський

Моделювання фізичних властивостей та експериментальних результатів для віртуального p-i-n діода на основі структури метал-ізолятор-кремній

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Вивчення фізичних процесів в конденсаторах ізолятор-напівпровідник (МІН) вказує на новий шлях використання цього відомого приладу як високочутливого оптичного датчика з гігантським внутрішнім підсиленням вхідного сигналу. Теоретично досліджено та експериментально розроблено нові CMOS оптичні датчики з структурою метал-ізолятор-напівпровідник. Фізичні властивості цих датчиків описуються з моделлю МІН конденсатора, де враховано існування збідненого на електрони шару, інверсного шару дірок обмеженої глибини, і можливої зміни властивостей шару n-напівпровідника. Між двома квазірівноважними модами виникає тимчасова дворівнева діагональна напруга. Цей тимчасовість використовується як для зберігання так і для зняття показів вхідного оптичного сигналу для кількісних вимірювань слабкого інфрачервоного випромінювання. Запропонована проста процедура зняття показів зчитування інтегрованої інформації з істотним підсиленням. На зчитуванні інформації опір шару n-напівпровідника сильно змінюється і структура MIS поводиться як віртуальний p-i-n-діод з подвійним переходом носіїв в n- шарі. Підсилення (або поточний коефіцієнт перетворення) визначається співвідношенням часів інтеграції і зчитування і рівне біля 10^4-10^5 при великих зовнішніх навантаженнях (> 10 кОм) та досягає значення 10^6 при невеликих навантаженнях (~100 кОм). Теоретична модель пояснює поведінку датчика через накопичення термо- та фотогенерованих носіїв. Чисельне моделювання добре узгоджується з експериментальними дослідженнями запропонованих датчиків.