Local Transistor Isolation Using Oxidized Porous Silicon

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Modern microelectronics technology characterized by a number of process parameters called design rules and technological constraints. In particular, for formation of CMOS VLSI with design rules 0.5 microns and below the depth of the dielectric insulation for elements should be the value of <500 nm. For this reason, due to historical trend of reducing temperature in fabrication process, traditional conventional LOCOS technology and its variations (PBZ, SWAMI, SILO, PELOX, NCL) at this stage do not meet the requirements of VLSI structures production with a high yield.

Method includes operations of chemical treatment of n-Si substrate, forming n-p$^+$-p structures, forming Si_3N_4 mask using high frequency sputter deposition in N-Ar plasma, lithography, forming wells using anisotropic plasmochemical etching, electrochemical anodizing, oxidization, etching of well bottom and local epitaxy of n doped Si into formed wells.

Special attention should be paid to electrochemical anodizing. It used to form isolation from p$^+$ under p layer. Electrochemical anodizing is conducted in potentiostatic regime in electrolyte that consists of (volume parts):

Sulfuric acid (95%) – 0.549;

Hydrofluoric acid (48%) – 0.376;

Hydrochloric acid (95%) – 0.028;

Acetic peroxyacid ≤ 0.047;

hydrochloric acid added for effective removing of H_2 bubbles and increasing of anodizing speed, and acetic peroxyacid causes qualitative wetting of the activated surface. Anodizing process is conducted on device for electrochemical anodizing “Pauk-2K” which has 6 cells for electrochemical anodizing. Porosity of Si is determined by current density (Fig. 1).

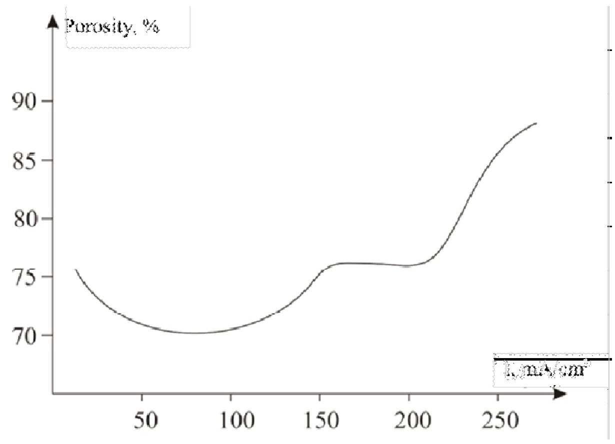

Fig. 1. Porosity of Si vs anodizing current density

Proposed process is easy to automatize for big diameter Si wafers (>150 mm)

Compared to isoplanar technology, proposed method leads to higher device density, higher performance, increased radiation hardness and temperature tolerance and reduced process variability.