Electrical diagnostics of h-k dielectrics on InGaAs

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Using of thin high-κ dielectric film materials in conjunction with III-V substrate is highly required for future progress and improvement of MOSFET performance in high speed logic and RF applications. In this work we present results of a study focused on electrical properties and determination of transport mechanism through dielectric layer in $Pd/Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ MOS system.

In the devices under study high-κ Al_2O_3 oxide layer was formed by atomic layer deposition (ALD) of nominal physical thickness t_{ox} of 5, 10, 15 and 20 nm. The top Pd gate metallization was obtained by a shadow mask process. The samples received no post-metallization annealing treatment. Samples with both *n*(S)- and *p*(Zn)- type doped ($4x10^{17}cm^{-3}$) $In_{0.53}Ga_{0.47}As$ epitaxial layers were characterized by capacitance-voltage (*C-V*), current-voltage (*I-V*) measurements over the temperature range of 100 – 300 K using an Agilent E4980A Precision LCR meter and Agilent 4156C Precision Semiconductor Parameter Analyzer.

The similarity of the *J-V* curves for both types of the substrates and the general shape of the characteristics are consistent with a current transport mechanism governed by electron tunneling through the triangular potential barrier at the metal-dielectric or semiconductor-dielectric interface. In both cases, the current can be described by Fowler-Nordheim (FN) tunneling mechanisms. For the case of electron tunneling from the metal electrode, the barrier height, φ_B, is the same for the 10, 15 and 20 nm thick dielectric and equals to 2.40±0.10 eV. For the electron tunneling from the semiconductor, 10 nm thick dielectric gives the barrier height φ_B =2.50±0.06 eV. This value represents the conduction-band energy offset at the Al_2O_3/InGaAs interface. The increase of the h-k dielectric thickness results in decrease of the burrier heigth.

Analysis of the *C-V* characteristics has demonstrated that Al_2O_3 deposited by ALD on $In_{0.53}Ga_{0.47}As$ surfaces exhibits a fixed positive charge distributed throughout the oxide. This positive charge would modify the barrier at the injecting interface resulting in an apparent reduction in the barrier height with increasing oxide thickness. It was found that no degradation and non-reversible charge trapping in the dielectric occurred. The evidence of the positive charge trapping also could be found from the shift of H-F *C-V* curve toward negative biases. Samples with thicker Al_2O_3 oxide demonstrate larger V_{fb} shift thus, the more charge captured in the oxide.

The model of the Al_2O_3/InGaAs transition layer transformation during the ALD process is proposed.