Modern Problems of CAD Topology Speed VLSI Structures

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Introduction

When designing the topology of high-speed VLSI structures used different methods. The main of them are:

- A manual calculation scheme for the previously prepared analytical calculation formulas of its elements;
- Physical modeling, ie the study of objects of a physical nature by means of objects having a second physical nature, but identical to the first mathematical description of the structure elements, based on the principles of physical modeling of electro analogies;
- Full-scale layout with elements and devices previously diluted PCB aided mathematical modeling using computers (PCs) using special software).

The disadvantage of a manual calculation circuit LSI and its topology - a low accuracy, limited functionality, inability to take account of parasitic effects (elements) and design rule design and technological constraints.

Physical modeling as a way of designing structures and CEA LSI is used very rarely, most often it is used for a detailed study of individual processes, such as heat, mathematical modeling which is rather complicated and time-consuming and is usually electrophysical diagnostics elements (processes).

Full-scale layout - is one of the oldest and common ways of designing REA, which under certain conditions can be transferred to WSI structure for ensuring maximum reliability of the results arising from work with real signals, devices, rather than their closest model. In addition, the full scale layout determines the appearance of the results in the form of options and features. Its main drawback - high cost of preparing a layout that provides development duration, limited prototyping in taking into account the actions of parasitic elements and processes, including transient.

For automated mathematical design on the PC usually refers to the full range of issues associated with all phases of design, functional, logical, schematic, technological, physical and topological, which created mathematical models that provide the full range of procedures for calculation, analysis, synthesis and optimization of topological solution with high density layout. Compared with other methods of automated mathematical modeling using modern software tools (Cadence, TCAD, PCAD, MATHCAD, MATLAB, Stalker, OTTO, OrCAD, MicroCap) has the following advantages.

In problems of calculating circuits using the model can always find the original settings circuits (including dynamic) and their characteristics that can not be measured directly in the layout because of the unavailability of

measurement points that are especially characteristic of high-speed VLSI structures.

In problems of modeling analysis allows to analyze the output parameters and characteristics of schemes boundary and over boundary modes that are physically impossible to implement, such as transients taking into account the actions of parasitic elements. In addition, the simulation allows you to calculate mass production and analysis of various statistical characteristics of the circuit without its launch in series production, analysis of the scheme of action of external conditions without real climatic tests using test electrophysical diagnostics, calculate hurt security schemes, and simulate analog-digital circuitry together.

In optimization problems possibility of technological model is limited by a small number of regulatory elements, while the new model can be varied parameters, achieving maximum improvement parameters and characteristics, especially speed. Optimization and minimization of elements in the scheme reduces power consumption and chip area, which increases the yield of VLSI structures.

The role of modeling in problems of synthesis allowed to clearly verify proper operations of synthesized circuits and topology taking into account the parasitic elements by minimizing their topological layout and routing.

Obviously, it is impossible to AC / VLSI and CEA varying degrees of difficulty to analyze and design with the same power of the detail, including at the processes that occur in each active element (transistor). Therefore, CAD design presents multi-hierarchical process. The content and the number of stages of the design depends on many factors, especially where there are features of an object and its ultimate goal of designing used electronic components and technologies of topology structures Mathematics (software) tools. As technology of VLSI structures CAD software tools should be improved in the shortest possible time to eliminate the above problems today.

References

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